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Referee report on the PhD Thesis

Placement and Routing for Dynamic Reconfiguration in FPGAs

written by Ing. Petr Honzík

The submitted thesis deals with the research in the field of reconfigurable computing. The research in this area began already in 1960 and has intensified in 1990s due to appearing of new architectures capable of dynamic reconfiguration - Field Programmable Gate Arrays (FPGAs). However, only a few architectures with partial dynamic reconfiguration capability, e.g., Xilinx Virtex-II family, which was introduced in 2001, and its followers achieved practical success. The main reason is lack of adequate design tools for dynamically reconfigurable systems and fast transitions between CMOS technology nodes making reconfiguration hardware platforms rapidly obsolete.

The thesis is based on three research projects solved by the Department of Signal Processing at UTIA AVČR in which the author has participated last seven years. The first and historically oldest part deals with the implementation of partial dynamic reconfiguration in FPGAs. There, the author analyzed complexity of reconfiguration process and contributed to implementation of reconfigurable coprocessors in two FPGA platforms: Atmel AT94K40FPSLIC and Xilinx XC2V1000. Although this topic was up-to-date at turn of the century, both architectures are now already matured. Therefore, this part of the thesis should be more focused on contemporary dynamically reconfigurable FPGAs and their impact on the performance of dynamically reconfigurable systems. Second part of the thesis, which is mainly based on the work of Daněk et al. (2008), deals with the design of self-adaptive element based on reconfigurable coprocessor and its verification in the ring bus topology. There, the author contributed to successful implementation of the network of self-adaptive elements acting as FIR filters, which was simulated in the MATLAB/Simulink environment and verified on Celoxica RC10 boards.

According to my opinion, the most important and the most up-to-date part of the thesis is the section dedicated to Networks on Chip (NoC), development of adequate placement and routing algorithms including self-adaptability features and their evaluation. In this section, one can trace the main contribution of the author who analyzed different NoC topologies, defined network cost parameters, developed three placement algorithms including the Step-Adaptive Algorithm, which improves placement of the running network, and implemented the simulation network where self-adaptive systems based on the mesh network were thoroughly tested. Although the proposed algorithms were mutually compared on different applications, I miss the detailed comparison with other published approaches and algorithms; consideration or introduction of other topological architectures suitable for NoC (Torus, Folded Torus, Hierarchical ring etc.), and consideration of additional criteria for NoC topology optimization (power consumption, reliability). Nevertheless, I can conclude that all objectives specified in the introduction of the thesis were successfully solved. The thesis contains quality original results and addresses recent topics in the field of NoC making the main contribution by acquiring new findings in the field of self-adaptive systems based on dynamic reconfiguration.

The thesis is written in good English, the proofs are clear and easily understandable. However, the author did not avoid some minor mistakes from which I regard as the most significant the incompleteness of some citations.

Conclusions

Summarizing all the above facts, I conclude that the submitted thesis fulfills the requirements for the PhD Thesis and meets standards of CTU Prague. I recommend the thesis to the defense and awarding the PhD degree to Ing. Petr Honzík.

Prague, December 6, 2010



Prof. Ing. Pavel Hazdra, CSc.