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Ph.D. Thesis Review

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Thema: Placement and Routing for Dynamic Reconfiguration in FPGAs

a) Characteristic and significance of the topic

The objective of the Thesis is building methods and techniques useful for static and dynamic reconfiguration of devices that are implemented in FPGA. The topic belongs to intensively studied problems in the past few years, because the possibility of reconfiguration of running devices which are implemented in modern FPGA comprises a wide range of opportunities to improve the reliability, fault-tolerance and also power consumption. The practical application of dynamic methods heavily depends on having effective configuration control systems and minimal reconfiguration overhead. Otherwise, the cost of control and reconfiguration overhead can offset any gains which are offered by the dynamic architecture. There exists huge number of papers at conferences like *FPL, Euromicro-Digital System Design Conference, Circuits and Systems Symposium, etc.* which deal with reconfiguration problems. Therefore the topic of the Thesis is current and relevant in the context of up-to-date research.

b) Satisfaction of the Thesis goals

The Thesis brings new ideas and practically usable scientific knowledge. The main goal of the Thesis is to design a self adaptive strategy of a reconfigurable computing unit and its partial verification by simulating several examples. The author also develops a design methodology for self adaptive placement of parts of the reconfigurable system and provides simulation of the placement algorithms. To my knowledge, this question has not been studied systematically yet, thus the topic of the paper is both interesting and new. The presented methodology seems to be useful and the goal of the Thesis can be considered fully satisfied.

c) The scientific methods used within the Thesis

The Thesis consists of seven chapters (Introduction, 5 Sections, Conclusions and three Appendices). It follows bibliography containing 60 items and a list of 22 author's publications (mostly as coauthor). The proposed reconfigurable architectures, using self adaptive placement methods and technologies are not presented just in the best form and I would say they are not described exhaustively. Parts of the authors work were simulated, some of them using his own simulation framework programmed in C++. The simulation results including their comparison are presented mostly in graphical form in appendices. The presented work is extensive; hence the Thesis is here and there very dense in information content. That said, I think some of the

most important concepts of the Thesis could be explained more clearly. At least I had troubles understanding the exact operation of the architecture during the adaptation process.

So, I have some critical remarks to the Thesis and I suppose that they should be discussed during the Thesis defence:

1. The dynamic reconfiguration analysis in Chapter 2 introduces two application types (stream-type applications and control applications). Does this classification cover all cases?
2. A formal one: The number of the figure at the beginning of the second paragraph on page 33 is probably wrong.
3. The bitstream organisation described in paragraph 3.2 distinguishes three possible organizations of configuration data. Isn't there any other way how to optimize the configuration process?
4. Does the adaptive reconfiguration algorithm consider the frame boundaries inside the device bitstream?
5. Is it possible to implement the bitstream relocation on the nowadays non homogenous FPGAs?
6. The programming model introduced in paragraph 3.2 on the page 40 supposes on demand transparent reconfiguration of the FPGA. Does it mean that some replacement algorithms are neccessary as they are during page fault in virtual memory (of course on very limited space)?
7. Can the exchange of dynamic units be predicted?
8. The author introduces some sensors in the paragraph 4.3 on page 54. The sensors should help to optimize the execution of loaded tasks. I miss at least a brief description of the sensor's exploitation. What parameters do they offer?
9. The network taxonomy which is described at the beginning of Chapter 5 brings no new knowledge and could be omitted. Perhaps the author's comments regarding the FPGA implementation are worth mentioning.
10. Chapter 4 of the Thesis introduces architecture of self-adapt element. I am missing any quantitative estimation of the cost (for example comparison of the chip area consumed by observer, controller, etc.).

The Thesis contains several good ideas that are often formulated in bad English, that appeares especially in the Doctoral Thesis Statement. Acording to my opinion the document like Ph.D. Thesis should be revised by a native speaker before publication.

The author's style of writing the Thesis lets the reader foresee that the work is a part of bigger research project involving more participants; the balance sheet is published as the last paragraph in the Chapter 7. I would appreciate it if I got this information at the beginning of the Thesis.

d) Results and outcomes with new information

The main contribution of the Thesis is the new developed methodology for placement and routing of dynamically reconfigurable functional blocks. The methodology is aimed for

improving the reliability and power consumption of such devices. From the implementation point of view it is considered a progressive FPGA technology for programmable electronic devices. The proposed methodology of the networking on chip is based on the standard graph model.

The contribution of this work is also a proposal of partial reconfiguration along with an extension of the current FPGA architecture to support such control reconfiguration using self adaptive placement. I find the idea novel and interesting. The simulation results also show significant savings in the area.

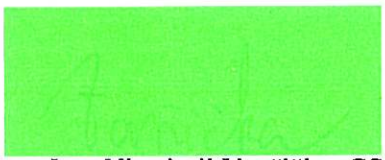
e) Applications and a contribution to the science progress

There are about 8 author's publications at prestigious international conferences and workshops that are related to the Thesis and also some publication at the national level. The work contributes to the improvement of properties of systems designed on the basis of FPGAs. The results of the Thesis can have direct positive impact on practical applications.

f) Overall evaluation – an overview

The Thesis reflects state of the arts and brings new results and outcomes in the form of publications. As stated, the published results were obtained during the work on following international projects: *Reconf 2*, *ATMEL Place & Route*, *Æther*, *Scalopes* and *C-A-K and C-A-K 2*.

The Thesis submitted by Ing. Petr Honzík fulfills the criteria of the §47 of the University education Act. No. 111/98 and § 32, Chapter 1 of the Regulations related to studying and examinations for the students of Czech Technical University of in Prague" and I recommend the Thesis for the Ph.D. defence.



Pilsen 12.11.2010

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